# Design Requirements

**Review & Approval:**

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| **Function** | **Name / Title** | **Signature** | **Date** |
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**Revision History:**

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| --- | --- | --- | --- |
| **Revision #** | **Description of Revision** | **Approval Date** | **Author** |
| 01 | Initial Release | 04/11/18 | BS |
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1. **Purpose/Scope:**

This document is part of design history file (DHF), this file is used to log the version history of change and log into detail the reason of change, the changes have been made and scope of improvement. This log is created and maintained at sub-project level.

The scope of this document only encompasses the design files, such as the mechanical, electrical and software design files, or any other design files that may contribute to the immediate design of the product. There shall be a separate log sheet for logging the versions for the other phases of the design and development process. The goal of this log is to provide a concise summary of all the design changes that were made to product design.

NOTE: Section 1, 2 are the guidelines for engineer usage, DO NOT edit or modify without template document version control. Section 3 and 4 are editable by the engineer, the Document number on the right up corner should be unique, ABV are the abbreviation of the project code. Reference Project Code Live Doc.docx

1. **Responsibilities:**

**Engineer:** Keep log the document, naming the document in version base. Update the log reversion time and file path, update the description of the update.

**Project Managers:** review the design history log file, and control the version of the log.

**Department Head:**  review the project managers’ report in progress.

1. **Related Information**

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| **Project Name:** | Canady Hybrid Plasma New Generator-T800 Project |
| **Project Code:** | PMLS-14-003 |
| **Project Abbreviation:** | PG |
| **Project Manager Name:** | Taisen Zhuang |
| **Engineer Name:** | Buddika Sumanasena |
| **Components/Subcomponents Name:** | Full Bridge Main Board, Full Bridge Controller Board, Power Supply Board |
| **Components/Subcomponents Part Number:** | PG\_SPC\_FBG\_001\_R001 |

1. **Design History Log**

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| **Document Number/Version Number/Revision Number** | **Descriptions: (Here put three or more key things, the reason of change, what has been changed, the results of modification)** | **Acted by:** |
| Rev A | Initial Release | Taisen Zhuang |
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1. **Design Requirement**

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| **5.1 Electrical Requirement** | This section will mainly specify the external electrical requirements for running the Full Bridge DC-DC Converter while meeting its functional requirements.  5.1.1 Input voltage of 369V-410V DC is required for this system to function. Ripple requirement: 10% Vp-p. This power source should provide maximum of 1.2A current.  5.1.3 Auxiliary power supply of 12V DC with 500mA maximum current capability.  5.1.4 FPGA interface for controlling the system-No external power supplies required from the FPGA.  5.1.5 FPGA interface and the auxiliary power supply should share a common ground.  5.1.6 Ensure that all mounting holes are floating with proper isolation to prevent ESD effects.  5.1.6 Power ground must be isolated from auxiliary GND. |
| **5.2 Mechanical Requirement** | 5.2.1 Main board size less than 170mm by 110mm.  5.2.1.1 Rounded corners with a radius of 1.27mm (system level).  5.2.2 Systems overall height should be less than 85mm. This includes the clearance to the bottom and the top.  5.2.3 Board Mounting.  5.2.3.1 The board should be mounted in such a way that it can handle the impact when the unit is dropped from 2m (derive from IEC60601-1) without impairment of its functionality.  5.2.3.2 Board standoffs need to be metallic.  5.2.3.3 The board should have atleast four mounting holes which can accommodate M4 screws with 7.2mm head diameter with lock washer.  5.2.3.3 Heat sink should be mounted with screws and should survive the unit been dropped 2m.  5.2.4 Connectors and cables:  5.2.4.1 All connectors should be dumb-proof.  5.2.4.2 All connectors should have locking feature to avoid loosening.  5.2.4.3 All power cables assemblies should adhere to standard color codes and have tubing for additional insulation.  5.2.4.4 Connectors and matching cable assemblies should be selected with DFM in mind.  5.2.10 Overall weight should be less than 1.2Kg.  5.2.11 Sub boards of the system should be mounted to the main board using assemblies that have locking features.  5.2.12 Consider adding zip ties on inductors. |
| **5.3 Functional Requirement** | For the system to be considered functional it must meet the following specifications.  5.3.2 Output power requirements.  5.3.2.1 The system should produce an output voltage adjustable between 10V and 100V. When the system is not operational, voltage should drop to zero.  5.3.2.2 Output voltage should be adjustable by steps less than 0.25V.  5.3.2.3 The system should be able to deliver atleast to 4.25A current at 100V with 20% current ripple at maximum.  5.3.2.4 The system should be able to deliver up to 425W.  5.3.2.5 Power efficiency of the system at maximum power delivery should be more than 90%.  5.3.2.6 Response time: In the system, response time will be calculated based on the time it takes to reach from minimum to maximum voltage and becomes stable. (Please consider Damping Ratio and percentage overshoot).  5.3.2.7 Adding capacitor clean up function to prevent output power overshoot to the patient.  5.3.2.8 Initial booting sequence time should not exceed 2s  5.3.2.9 In-system booting sequence time should not exceed 5ms  5.3.2.10 Low to high power- No clean up capacitor feature required.  High to low power- Activate clean up feature.  Clean up capacitor feature should only be used during setup and not during active surgery.  5.3.2.11 Initialization function test: Includes testing the input voltage, auxiliary input voltage, output voltage.  5.3.3 Isolation requirements:  5.3.3.1 Input and output power lines should be isolated up to 2.5KV  5.3.3.2 Input and output power lines should be isolated from Auxiliary power supply and the FPGA interface by at least 3KV. (Constraint Comes from isolated power supply)  5.3.4 Detection features.  5.3.4.1 The system should detect the FPGA interface when the power input voltage falls outside the 369V-410V range.  5.3.4.2 The system should detect the FPGA interface when the auxiliary power supply is out of the 10V-14V range.  5.3.4.3 The system should detect the FPGA interface overcurrent conditions.  5.3.4.4 The system should provide the FPGA controller a mechanism to turn off the main power input if a fault condition occurs.  5.3.5 Output voltage measurement.  5.3.5.1 The output voltage of the system should be readable via the FPGA interface.  5.3.5.2 Output voltage can be measured at 1KHz frequency.  5.3.5.3 Output voltage measurement has at least 5% accuracy.  5.3.6 The system should keep the Inrush Current Limiting within safe limits.  5.3.7 Startup of the system should not electrically stress any of its power components.  5.3.8 The system should have status indication using LEDs when connected to the FPGA.  5.3.9 Heatsink temperature should not increase by more than 50C when operated with full power for 1 hour.  5.3.10 Test Requirements: Plenty of test points as per manufacturing/ assembly/maintenance testing procedure. Ensure the TPs are easily visible and accessible. |
| **5.4 Safety Requirement** | 5.4.1 The system should be normally off.  5.4.2 The full bridge function should be disabled when the FPGA is disconnected from the system.  5.4.3 The system should have a fast acting fuse with a minimum requirement of 1.5A for the power input.  5.4.4 The system must function at the stated operating temperature and humidity levels (Receive from system level requirements).  5.4.5 Adding a slot between the Input connector pins to add more isolation.  5.3.4 Detection features.  5.3.4.1 The system should detect and control the FPGA interface when the power input voltage falls outside the 369V-410V range.  5.3.4.2 The system should detect and control the FPGA interface when the auxiliary power supply is out of the 10V-14V range.  5.3.4.3 The system should detect and control the FPGA interface overcurrent conditions.  5.3.4.4 The system should provide the FPGA controller a mechanism to turn off the main power input if a fault condition occurs. |
| **5.5 Manufacture Requirement** | 5.5.1 PCB manufacturing requirements.  5.5.1.1 Main board size 160mmx100mm.  5.5.1.2 All boards of the system are of matte black color.  5.5.1.3 Main board should be of 2mm thickness and have at least 1oz copper thickness in all layers.  5.5.1.4 Control sub board and power supply sub board should be of 1.6mm thickness and have 1oz copper thickness in outer layers and at least 0.5oz copper thickness in inner layers.  5.5.1.5 The PCB manufacturing facility should have at least 6mil clearance and 12mil hole capability.  5.5.1.6 Lead free HASL or ENIG surface finishing should be used for PCB.  5.5.1.7 Have a method to lock the screws in place: screw washer and/or glue. |
| **5.6 Label Requirement** | 5.6.1 PCB labeling: Specify high voltage label symbol on silk screen  5.6.2 All voltage labeled on the silk screen.  5.6.3 All key Test points required for Testing and manufacturing should be labeled for better readability.  5.6.4 All PCB boards must have Logo on the silk screen.  5.6.5 All connectors should be labeled  5.6.6 Each board must be labeled with product code derived from the technical numbering structure document.  5.6.7 Manufacturing lot number on each PCB board for better traceability.  5.6.8 Manufacturing factory test pass label-Not required on each board.  5.6.9 Each cable must have its unique label for tracking purposes. |
| **5.7 Software Requirements:** | 5.7.1 Always use Verilog HDL when coding the FPGA  5.7.2 CLK requirement from system level:  Cannot use clock faster than 50MHz for data interfaces.  5.7.4 Data Enable/Disable  5.7.5 Reset feature: Always reset to default condition for all parameters and register. Reset is level triggered by low level.  5.7.6 Consider using initial function in your Verilog code.  5.7.7 Consider using data valid condition sending to the FPGA:  5.7.8 Define all sub system level error conditions. |
| **5.8 Regulatory Requirements and Standards** | 5.7.1 System level |
| **5.8 Material biocompatibility:** | 5.8.1 All electrical and mechanical components used within the sub system must be ROHS compliant. |
| **5.9 Packaging and Shipping Requirement:** |  |
| **5.10 Legal Requirement:** | **N/A *(Only applicable on a system level)*** |
| **5.11 Storage and Shelf Life:** |  |
| **5.12 Clinical Requirement:** | **N/A *(Only applicable on a system level)*** |
| **5.13 Training Requirement:** | **N/A *(Only applicable on a system level)*** |
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